

## Refine Search

### Search Results -

| Term  | Documents |
|---|-----------|
| TAKEN   | 2307757   |
| TAKENS  | 64        |
| CONCURRENT\$4   | 0         |
| CONCURRENT  | 93441     |
| CONCURRENTCY  | 1         |
| CONCURRENTELY   | 1         |
| CONCURRENTTEST  | 1         |
| CONCURRENTFLOW  | 1         |
| CONCURRENTIE  | 1         |
| CONCURRENTIT  | 1         |
| CONCURRENTIY  | 4         |
| ((((CONCURRENT\$4 OR SIMULTANEOUS\$3 OR PARALLEL\$7) NEAR8 EXECUT\$3 AND (FETCH\$5 OR PREFETCH\$5) AND BRANCH\$5 NEAR10 DECOD\$4 AND TAKEN AND (INHIBIT\$4 OR HALT\$4 OR CANCEL\$5 OR SUSPEND\$3 OR SUSPENSION\$1) NEAR8 (INSTRUCTION\$1 OR MICROINSTRUCTION\$1 OR MACROINSTRUCTION\$1) AND IDENTIF\$7).CLM.).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD. | 1         |

There are more results than shown above. [Click here to view the entire set.](#)

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
 JPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L36

[Refine Search](#)

[Recall Text](#)

[Clear](#)

[Interrupt](#)

### Search History

DATE: Thursday, August 17, 2006   [Printable Copy](#)   [Create Case](#)

| <u>Set</u><br><u>Name</u>                                     | <u>Query</u>   | <u>Hit</u><br><u>Count</u> | <u>Set</u><br><u>Name</u><br>result<br>set |
|---|--|----------------------------|--|
| <i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i> |  |                            |  |
| <u>L36</u>  | ((concurrent\$4 or simultaneous\$3 or parallel\$7) near8 execut\$3 and (fetch\$5 or prefetch\$5) and branch\$5 near10 decod\$4 and taken and (inhibit\$4 or halt\$4 or cancel\$5 or suspend\$3 or suspension\$1) near8 (instruction\$1 or microinstruction\$1 or macroinstruction\$1) and identif\$7).clm. | 1                          | <u>L36</u>                                 |
| <u>L35</u>  | ((fetch\$5 or prefetch\$5) and branch\$5 near10 decod\$4 and taken and (inhibit\$4 or halt\$4 or cancel\$5 or suspend\$3 or suspension\$1) near8 (instruction\$1 or microinstruction\$1 or macroinstruction\$1) and identif\$7).clm.   | 3                          | <u>L35</u>                                 |
| <u>L34</u>  | L33 not l9   | 3                          | <u>L34</u>                                 |
| <u>L33</u>  | L32 and l8   | 356                        | <u>L33</u>                                 |
| <u>L32</u>  | L31 and l4   | 426                        | <u>L32</u>                                 |
| <u>L31</u>  | (inhibit\$4 or halt\$4 or cancel\$5 or suspend\$3 or suspension\$1) near8 (instruction\$1 or microinstruction\$1 or macroinstruction\$1)   | 14105                      | <u>L31</u>                                 |
| <i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>                          |  |                            |  |
| <u>L30</u>  | l10 and l15  | 12                         | <u>L30</u>                                 |
| <u>L29</u>  | l10 and l14  | 68                         | <u>L29</u>                                 |
| <u>L28</u>  | l10 and l13  | 7                          | <u>L28</u>                                 |
| <u>L27</u>  | l10 and l12  | 77                         | <u>L27</u>                                 |
| <u>L26</u>  | l10 and l11  | 228                        | <u>L26</u>                                 |
| <u>L25</u>  | l9 and l15   | 16                         | <u>L25</u>                                 |
| <u>L24</u>  | l9 and l14   | 83                         | <u>L24</u>                                 |
| <u>L23</u>  | l9 and l13   | 12                         | <u>L23</u>                                 |
| <u>L22</u>  | l9 and l12   | 100                        | <u>L22</u>                                 |
| <u>L21</u>  | l9 and l11   | 292                        | <u>L21</u>                                 |
| <u>L20</u>  | l7 and l15   | 18                         | <u>L20</u>                                 |
| <u>L19</u>  | l7 and l14   | 95                         | <u>L19</u>                                 |
| <u>L18</u>  | l7 and l13   | 15                         | <u>L18</u>                                 |
| <u>L17</u>  | l7 and l12   | 113                        | <u>L17</u>                                 |
| <u>L16</u>  | l7 and l11   | 340                        | <u>L16</u>                                 |
| <u>L15</u>  | (711/213)[CCLS]  | 457                        | <u>L15</u>                                 |
| <u>L14</u>  | (712/23,41)[CCLS]  | 841                        | <u>L14</u>                                 |
| <u>L13</u>  | (712/245-248)[CCLS]  | 794                        | <u>L13</u>                                 |
| <u>L12</u>  | (712/23-43, 208-240)![CCLS]  | 3391                       | <u>L12</u>                                 |
| <u>L11</u>  | (712/2-300)[CCLS]  | 12464                      | <u>L11</u>                                 |
| <i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i> |  |                            |  |
| <u>L10</u>  | L9 and branch\$3 near8 decod\$3  | 264                        | <u>L10</u>                                 |
| <u>L9</u>   | L8 and l7  | 353                        | <u>L9</u>                                  |
| <u>L8</u>   | (identif\$6 or id) near8 (instruction\$1 or microinstruction\$1 or macroinstruction\$1)  | 36602                      | <u>L8</u>                                  |

|           |   |       |           |
|-----------|---|-------|-----------|
| <u>L7</u> | L6 and l4   | 420   | <u>L7</u> |
| <u>L6</u> | L5  | 13605 | <u>L6</u> |
| <u>L5</u> | (inhibit\$4 or halt\$4 or cancel\$5 or suspend\$3 or syspension\$1) near8<br>(instruction\$1 or microinstruction\$1 or macroinstruction\$1) | 13605 | <u>L5</u> |
| <u>L4</u> | L3 and l2   | 1087  | <u>L4</u> |
| <u>L3</u> | (fetch\$5 or prefetch\$5) and (branch\$4) near7 (predict\$5 or speculat\$5) near25<br>taken   | 1747  | <u>L3</u> |
| <u>L2</u> | (concurrent\$4 or simultaneous\$3 or parallel\$7) near8 execut\$3   | 66419 | <u>L2</u> |
| <u>L1</u> | (fetch\$5 or prefetch\$5) and (branch\$4) near7 (predict\$5 or speculat\$5)   | 4203  | <u>L1</u> |

END OF SEARCH HISTORY


[Home](#) | [Login](#) | [Logout](#) | [Access information](#) | [All](#)

Welcome United States Patent and Trademark Office

Search Results

[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "(((fetch\*, prefetch\*) &lt;and&gt; (branch\*) &lt;near/10&gt; decod\* &lt;and&gt; taken)&lt;in&gt;met..."

e-mail

Your search matched 2 of 1392165 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

[View Session History](#)[New Search](#)

Modify Search

(((fetch\*, prefetch\*) &lt;and&gt; (branch\*) &lt;near/10&gt; decod\* &lt;and&gt; taken)&lt;in&gt;metadata)

[Search](#)☐ Check to search only within this results set

» Key

Display Format:



Citation



Citation &amp; Abstract

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

[view selected items](#)[Select All](#) [Deselect All](#)**1. Control speculation for energy-efficient next-generation superscalar processors**

Aragon, J.L.; Gonzalez, J.; Gonzalez, A.;

[Computers. IEEE Transactions on](#)

Volume 55, Issue 3, March 2006 Page(s):281 - 291

Digital Object Identifier 10.1109/TC.2006.32

**Summary:** Conventional front-end designs attempt to maximize the number of "in-flight" instruction. However, branch mispredictions cause the processor to fetch useless instructions that are eventually increasing front-end energy and .....[AbstractPlus](#) | Full Text: [PDF](#)(3552 KB) IEEE JNL[Rights and Permissions](#)**2. Power-aware control speculation through selective throttling**

Aragon, J.L.; Gonzalez, J.; Gonzalez, A.;

[High-Performance Computer Architecture, 2003. HPCA-9 2003. Proceedings. The Ninth International Conference on](#)

8-12 Feb. 2003 Page(s):103 - 112

Digital Object Identifier 10.1109/HPCA.2003.1183528

**Summary:** With the constant advances in technology that lead to the increasing of the transistor clock frequency, power dissipation is becoming one of the major issues in high-performance processors. They increase their clock frequency.....[AbstractPlus](#) | Full Text: [PDF](#)(428 KB) IEEE CNF[Rights and Permissions](#)[Help](#) [Contact Us](#) [Privacy](#)

© Copyright 2006 IEEE

Indexed by  
 Inspec